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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,838	GALEOTOS ET AL.	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-15 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-15, 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1, 3-15, 17-23 have been examined.

Acknowledgment of papers filed: remarks and amendments filed on 04 January 2008.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-5, 7, 10, 12-15, 17, 18, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahalingaiah (U.S. Patent No. 5,960,467) in view of Gandhi (U.S. Patent No. 6,263,354) in further view of Meier (U.S. Patent No. 6,405,305).

4. Regarding claim 1, Mahalingaiah discloses a processor comprising: an address generator (col 3 line 57) configured to generate speculative data addresses (col 3 lines 57-61) in response to an address operand (col 3 lines 58-59) and one or more address parameters (col 3 lines 20-24); a pipelined execution unit configured to execute instructions in an instruction pipeline having a plurality of stages (col 9 line 58) using data at locations specified by the speculative data addresses (col 6 lines 38-47); a speculative register file (fig 3 reference 35) configured to hold the speculative data addresses as corresponding instructions advance through the execution unit (col 6 lines 38-47); an architectural register file (fig 1 reference 30) configured to hold architectural data addresses (col 20 lines 50-52); and control logic configured to write

speculative data addresses to the speculative register file (fig 1) as the speculative data addresses are generated by the address generator (abstract)

And to supply speculative data addresses and architectural data addresses to the address generator (abstract).

Mahalingaiah fails to disclose the use of a digital signal processor.

Gandhi discloses the use of a DSP (col 1 lines 45-47)

The invention of Mahalingaiah is regarding a speculative address technique used to speed up a processor. Mahalingaiah would likely be motivated to implement other techniques that result in speed increases as well. As disclosed by Gandhi col 1 lines 50-53, "a 'host DSP' is a general-purpose DSP designed to accomidate a wide range of processing applications. As such, it offers a speed increase over general-purpose computers. Additionally, it offers a low cost implementation (col 1 lines 65). Mahalingaiah would be clearly motivated to implement the use of a digital signal processor for these reasons.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the invention of Mahalingaiah and implement the speculative technique using a DSP rather than a typical CPU.

Mahalingaiah/Gandhi fails to disclose the result of the speculative registers once they become committed to an architectural state.

Meier discloses using pointers and renaming schemes to allow the speculative register to become architectural (col 18 lines 23-33)

Meier discloses two techniques for causing the speculative registers to become architectural; each has its advantages and disadvantages. Mahalingaiah/Gandhi would have been

motivated to utilize the pointer technique to save power and, in some cases, the time required to complete a transfer.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Mahalingaiah/Gandhi and allow it to use a pointer system described in Meier to hold the architectural register in the speculative register file.

5. Regarding claim 3, Mahalingaiah/Gandhi/Meier discloses a digital signal processor as defined in claim 2, further comprising an architectural register file configured to hold architectural data addresses, wherein the control logic is configured to move architectural data addresses from the speculative register file to the architectural register file in the event of a conflict for use of the speculative register file (col 20 lines 50-52).

6. Regarding claim 4, Mahalingaiah/Gandhi/Meier discloses a digital signal processor as defined in claim 3, wherein the control logic is configured to write speculative data addresses to successive slots in the speculative register file (col 7 lines 7-18).

Note that the ESP address in particular is a stack pointer, suggesting that the addresses are written in a stack format, which means the address are written successively.

7. Regarding claim 5, Mahalingaiah/Gandhi/Meier discloses a digital signal processor as defined in claim 4, wherein the control logic is configured to increment a pointer to a next available slot in the speculative register file (col 7 lines 7-18).

8. Regarding claim 7, Mahalingaiah/Gandhi/Meier discloses a digital signal processor as defined in claim 3, wherein the control logic is configured to mark as architectural an entry in the speculative register file in response to the corresponding instruction being completed by the pipelined execution unit (col 18 lines 5-14).

9. Regarding claim 10, Mahalingaiah/Gandhi/Meier discloses a digital signal processor as defined in claim 1, wherein the control logic is configured to update a control register corresponding to the one or more address parameters when a speculative data address is written to the speculative register file (col 3 lines 20-24).

Note that since these addresses are generated using multiple operands, clearly for the program to progress these parameters have to be updated. And clearly, some type of "control logic" is used to configure this update to what can be referred to as a "control register". The use of assigning names to these particular features does not differentiate them from features in the referenced invention.

10. Regarding claim 12, Mahalingaiah/Gandhi/Meier discloses a digital signal processor as defined in claim 1, wherein the speculative register file has more slots than a number of pipeline stages in the pipelined execution unit (col 3 lines 37-42 and col 7 lines 7-15).

Note that the first citation states that the execution occurs on a second clock cycle, suggesting that there is only 1 clock cycle or one stage (see col 1 lines 17-21) for the execution unit. Additionally, the use of the term "register file" suggests many register slots, particularly since a stack pointer is necessary. Examiner asserts that there must be at least three register

slots (two more than the number of execution stages) in order to require a stack to organize the register file.

11. Regarding claim 13, Mahalingaiah/Gandhi/Meier discloses a digital signal processor as defined in claim 1, wherein the speculative register file has two more slots than a number of stages in the pipelined execution unit (Combine with 12).

12. Regarding claim 14, Mahalingaiah/Gandhi/Meier discloses a method for operating a digital signal processor, comprising: generating a speculative data address (col 3 lines 57-61) in response to an address operand (col 3 lines 58-59) and one or more address parameters (col 3 lines 20-24); executing an instruction using data at a location specified by the speculative data address (col 6 lines 38-47) in a pipelined execution unit (col 9 line 58); holding the speculative data address in a speculative register file as a corresponding instruction advances through the pipeline (col 6 lines 38-47); holding one or more speculative data addresses that have become architectural data addresses in the speculative register file (Meier col. 18 lines 23-33) and writing the speculative data address (fig 1) to the speculative register file as the speculative data address is generated by the address generator (abstract--see claim 1).

13. Regarding claim 15, Mahalingaiah/Gandhi/Meier discloses a method as defined in claim 14, further comprising: holding architectural data addresses in an architectural register file (col 20 lines 50-52), moving an architectural data address from the speculative register file to the

architectural register file in the event of a conflict for use of the speculative register file (col 20 lines 50-52).

14. Regarding claim 17, Mahalingaiah/Gandhi/Meier discloses a method as defined in claim 14, further comprising generating a next speculative data address based on a current speculative data address (col 1 lines 28-30).

Note that a program, as cited, has a sequential list of instructions. Clearly the next instruction speculatively chosen will depend on the current instruction.

15. Regarding claim 18, Mahalingaiah/Gandhi/Meier discloses a method as defined in claim 14, further comprising marking as architectural an entry in the speculative register file when a corresponding instruction is completed by the pipelined execution unit (col 18 lines 5-14).

16. Regarding claim 21, Mahalingaiah/Gandhi/Meier discloses a method as defined in claim 14, further comprising updating a control register corresponding to the one or more address parameters when the speculative data address is written to the speculative register file (col 3 lines 20-24).

Note: see claim 10

17. Claims 6, 8, 9, 11, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahalingaiah/Gandhi/Meier in view of Energy-Effective Issue Logic (herein EEIL).

18. Regarding claim 6, Mahalingaiah/Gandhi/Meier discloses a digital signal processor as defined in claim 5.

Mahalingaiah/Gandhi/Meier fails to disclose a circular buffer configured to wrap the pointer from one end of the register file to the start.

EEIL discloses a circular buffer having a head and tail pointer (EEIL fig 2 on page 234).

It is expected that one of ordinary skill in the art would have appreciated that a circular queue is a low-energy mechanism for storing registers that still maintains a reasonable amount of versatility. In the second column of page 234, EEIL states advantages over certain techniques: "collapsing makes a more effective use of the instruction queue but is much more energy demanding since collapsing implies a shift of all the entries between the tail and the empty entry". Mahalingaiah/Gandhi/Meier would clearly be motivated to utilize this method to save power.

It would have been obvious at the time of the invention for one of ordinary skill in the art to implement the circular queue of EEIL as the speculative register in the system of Mahalingaiah/Gandhi/Meier.

19. Regarding claim 8, Mahalingaiah/Gandhi/Meier/EEIL discloses a digital signal processor as defined in claim 7, wherein the control logic is configured to mark as empty a slot in the speculative register file containing an old architectural data address when a current architectural data address is defined (EEIL fig 2).

Note that the area outside of the head and tail pointer is considered to be an "empty area".

20. Regarding claim 9, Mahalingaiah/Gandhi/Meier/EEIL discloses a digital signal processor as defined in claim 7, wherein the control logic is configured to mark as empty a slot (EEIL fig 2—see claim 8) in the speculative register file when the speculative data address stored therein does not become an architectural data address (col 9 line 66 to col 10 line 2).

21. Regarding claim 11, Mahalingaiah/Gandhi/Meier/EEIL discloses a digital signal processor as defined in claim 1, wherein the speculative register file comprises a circular buffer (see claim 6).

22. Regarding claim 19, Mahalingaiah/Gandhi/Meier/EEIL discloses a method as defined in claim 14, further comprising marking as empty a slot (EEIL fig 2—see claim 8)in the speculative register file containing an old architectural data address when a current architectural data address is defined (col 9 line 66 to col 10 line 2 and col 18 lines 5-14).

Note that the instruction addresses are considered architectural when they are retired; however, the first citation states that these values can be invalidated--which would mark the slot as empty.

23. Regarding claim 20, Mahalingaiah/Gandhi/Meier/EEIL discloses a method as defined in claim 14, further comprising marking as empty a slot (EEIL fig 2—see claim 8) in the speculative register file when a speculative data address contained therein does not become an architectural data address (col 9 line 66 to col 10 line 2).

24. Claims 22 and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Mahalingaiah/Gandhi/Meier in view of common art.

Regarding claims 22 and 23, Mahalingaiah/Gandhi/Meier discloses the invention of claims 1 and 14, but fails to disclose that the speculative register information is copied to the architectural register once the speculative register file becomes full. Meier does disclose the technique of copying, but not necessarily in this circumstance (col 18 lines 23-33)

Examiner takes Official Notice that it is common in the art to copy renamed register information into its appropriate register when the renamed register becomes full.

Examiner asserts that this technique only makes sense. Rather than cause stalls in the processing system until a particular register file has available memory space, Mahalingaiah/Gandhi/Meier would have been motivated to copy the information to it's appropriate architectural register.

It would have been obvious at the time of the invention for the computing system of Mahalingaiah/Gandhi/Meier to copy architectural register information from the speculative register to the architectural register when the speculative register file becomes full.

Response to Arguments

25. Applicant's arguments filed 04 January 2008 have been fully considered but they are not persuasive.

26. Applicant has clarified the claim language in amendment and remarks. The following is a summary of Applicant's arguments, as Examiner understands them. Applicant has stated that the claimed speculative registers correspondence with the processor is limited to the quantity of registers. In particular, the number of registers must be equal or greater than the number of pipeline stages within the execution unit. Applicant claims that Mahalingaiah, Gandhi and Meier fail to disclose this limitation. Applicant also notes that the addition of Meier limits the number of speculative registers that the combined reference is capable of holding, because the speculative registers are converted to architectural registers. Furthermore, Applicant notes that Mahalingaiah's speculative register file is disclosed to be the size of the reorder buffer, which is shown in some detail in figures 4, 4A and 4B of Mahalingaiah.

This argument is unpersuasive. Applicant has clarified that the number of entries in the speculative register file must be equal or greater than the number of pipeline stages in the execution unit. This execution unit, as far as Examiner can determine, is no more than an arbitrary label placed on a certain plurality of processor stages. Such a label can be easily put on two arbitrary pipeline stages within the combined reference, as long as remaining limitations of the claim are satisfied. Here, it appears that the execution unit must contain a plurality of stages. Consequently, two stages within the combined reference are interpreted by Examiner to be part of the claimed execution unit.

The claim limitations require, therefore, that the speculative register file be capable of carrying two speculative addresses. The figures 4, 4A and 4B appear to indicate that the speculative register file can contain at least 4 entries. Four is, of course, larger than two and

there are even two entries available to be converted to an architectural address (with the addition of Meier) as required by the claims.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183